REMARKS

The Official Action mailed June 18, 2002 has been received and its contents carefully noted. Filed concurrently herewith is a *Request for a Third-Month Extension of Time*, which extends the shortened statutory period for response to July 23, 2003. Accordingly, Applicant respectfully submits that this response is being timely filed.

Applicant notes with appreciation the consideration of the Information Disclosure Statements filed on November 12, 1998, December 17, 1998, October 10, 2000, January 3, 2001, March 12, 2001, August 24, 2001, September 24, 2001, May 13, 2002, and November 6, 2002. A further Information Disclosure Statement is submitted herewith and careful review and consideration of this IDS is requested.

Claims 1-25, 34-39, and 41-42 are now pending in the present application, of which claims 1, 6, 11, 16, 19, 37 and 42 are independent. The independent claims have been amended to better recite the features of the present invention. For the reasons set forth in detail below, all claims are believed to be in condition for allowance.

A broad concept of the present invention is a semiconductor device that includes an active matrix circuit having at least one first thin film transistor, and a driving circuit having at least one second thin film transistor, each of the first and second thin film transistors comprising a semiconductor film including a channel forming region, a pair of first regions containing an impurity for giving one conductivity type thereto with the channel forming region therebetween, and a pair of second regions in which a concentration of the impurity is smaller than that in the first regions, wherein the second regions are interposed between the channel forming region and the pair of first regions, and wherein a distance between edges of the channel forming region and edges of the pair of first regions of the first thin film transistor is greater than that of the second thin film transistor.

Paragraph 2 of the Official Action rejects claims 1-4, 6-9, 12-14, 16-22, 24, 25, 34-38, 41 and 42 as obvious based on the combination of U.S. Patent No. 5,323,042 to Matsumoto and U.S. Patent No. 5,412,493 to Kunii et al. The Applicants respectfully submit that a *prima facie* case of obviousness cannot be maintained against the independent claims of the present invention, as amended.

The prior art, either alone or in combination, does not teach or suggest all the features of the independent claims, as amended. The independent claims of the present invention have been amended to recite that a distance between edges of the channel forming region and edges of the pair of first regions of the first thin film transistor is greater than that of the second thin film transistor. Matsumoto and Kunii do not teach or suggest at least this feature of the present invention.

Furthermore, the Applicants respectfully submit that the Official Action has not addressed Applicants' argument presented in the Amendment filed May 23, 2003, namely that Matsumoto and Kunii do not teach or suggest any relation between a length of a low level impurity region of a first TFT of an active matrix circuit and that of a second TFT in a driver circuit.

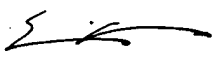
Since Matsumoto and Kunii do not teach or suggest all the claim limitations, a *prima facie* case of obviousness cannot be maintained. Accordingly, reconsideration and withdrawal of the rejection under 35 U.S.C. § 103(a) are in order and respectfully requested.

Paragraphs 3-5 of the Official Action reject claims 5, 10, 11, 15, 23 and 39 as obvious based on the combination of Matsumoto, Kunii and either U.S. Patent No. 5,028,551 to Dohjo et al., U.S. Patent No. 5,430,320 to Lee, or JP 56-40269 to Iizuka. Either Dohjo, Lee or Iizuka does not cure the deficiencies in Matsumoto and Kunii. As noted in the Amendment filed May 23, 2003, the Official Action relies on Dohjo, Lee and Iizuka to allegedly teach features which are not related to a distance between edges of the channel forming region and edges of the pair of first regions of the first thin film transistor is greater than that of the second thin film transistor. Matsumoto, Kunii and either Dohjo, Lee or Iizuka, either alone or in combination, do not teach or suggest either a distance between edges of the channel forming region and edges of the pair of first regions of the first thin film transistor is greater than that of the second thin film transistor, or any relation between a length of a low level impurity region of a first TFT of an active matrix circuit and that of a second TFT in a driver circuit. Since Matsumoto, Kunii and either Dohjo, Lee or Iizuka do not teach or suggest all the claim limitations, a *prima facie* case of obviousness cannot be maintained. Accordingly, reconsideration

and withdrawal of the rejection under 35 U.S.C. § 103(a) are in order and respectfully requested.

Should the Examiner believe that anything further would be desirable to place this application in better condition for allowance, the Examiner is invited to contact Applicant's undersigned attorney at the telephone number listed below.

Respectfully submitted,



Eric J. Robinson
Reg. No. 38,285

Robinson Intellectual Property Law Office, P.C.
PMB 955
21010 Southbank Street
Potomac Falls, Virginia 20165
(571) 434-6789